=========================================================================

\* Design Summary \*

=========================================================================

Top Level Output File Name : register\_bank.ngc

Primitive and Black Box Usage:

------------------------------

# BELS : 65

# GND : 1

# LUT6 : 64

# RAMS : 14

# RAM32M : 10

# RAM32X1D : 4

# Clock Buffers : 1

# BUFGP : 1

# IO Buffers : 112

# IBUF : 48

# OBUF : 64

Device utilization summary:

---------------------------

Selected Device : 6slx9tqg144-3

Slice Logic Utilization:

Number of Slice LUTs: 112 out of 5720 1%

Number used as Logic: 64 out of 5720 1%

Number used as Memory: 48 out of 1440 3%

Number used as RAM: 48

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 112

Number with an unused Flip Flop: 112 out of 112 100%

Number with an unused LUT: 0 out of 112 0%

Number of fully used LUT-FF pairs: 0 out of 112 0%

Number of unique control sets: 0

IO Utilization:

Number of IOs: 113

Number of bonded IOBs: 113 out of 102 110% (\*)

Specific Feature Utilization:

Number of BUFG/BUFGCTRLs: 1 out of 16 6%

WARNING:Xst:1336 - (\*) More than 100% of Device resources are used

---------------------------

Partition Resource Summary:

---------------------------

No Partitions were found in this design.

---------------------------

=========================================================================

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT

GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

------------------

-----------------------------------+------------------------+-------+

Clock Signal | Clock buffer(FF name) | Load |

-----------------------------------+------------------------+-------+

clk | BUFGP | 14 |

-----------------------------------+------------------------+-------+

Asynchronous Control Signals Information:

----------------------------------------

No asynchronous control signals found in this design

Timing Summary:

---------------

Speed Grade: -3

Minimum period: No path found

Minimum input arrival time before clock: 2.802ns

Maximum output required time after clock: 5.217ns

Maximum combinational path delay: 7.256ns

Timing Details:

---------------

All values displayed in nanoseconds (ns)

=========================================================================

Timing constraint: Default OFFSET IN BEFORE for Clock 'clk'

Total number of paths / destination ports: 168 / 168

-------------------------------------------------------------------------

Offset: 2.802ns (Levels of Logic = 1)

Source: readRegister1<4> (PAD)

Destination: Mram\_mem71 (RAM)

Destination Clock: clk rising

Data Path: readRegister1<4> to Mram\_mem71

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

IBUF:I->O 49 1.222 1.533 readRegister1\_4\_IBUF (readRegister1\_4\_IBUF)

RAM32X1D:DPRA4 0.047 Mram\_mem71

----------------------------------------

Total 2.802ns (1.269ns logic, 1.533ns route)

(45.3% logic, 54.7% route)

=========================================================================

Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'

Total number of paths / destination ports: 64 / 64

-------------------------------------------------------------------------

Offset: 5.217ns (Levels of Logic = 2)

Source: Mram\_mem6 (RAM)

Destination: readData1<27> (PAD)

Source Clock: clk rising

Data Path: Mram\_mem6 to readData1<27>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

RAM32M:WCLK->DOB1 1 0.920 0.944 Mram\_mem6 (readRegister1[4]\_read\_port\_1\_OUT<27>)

LUT6:I0->O 1 0.203 0.579 Mmux\_readData1201 (readData1\_27\_OBUF)

OBUF:I->O 2.571 readData1\_27\_OBUF (readData1<27>)

----------------------------------------

Total 5.217ns (3.694ns logic, 1.523ns route)

(70.8% logic, 29.2% route)

=========================================================================

Timing constraint: Default path analysis

Total number of paths / destination ports: 340 / 64

-------------------------------------------------------------------------

Delay: 7.256ns (Levels of Logic = 4)

Source: readRegister1<0> (PAD)

Destination: readData1<31> (PAD)

Data Path: readRegister1<0> to readData1<31>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

IBUF:I->O 49 1.222 1.533 readRegister1\_0\_IBUF (readRegister1\_0\_IBUF)

RAM32X1D:DPRA0->DPO 1 0.205 0.944 Mram\_mem71 (readRegister1[4]\_read\_port\_1\_OUT<30>)

LUT6:I0->O 1 0.203 0.579 Mmux\_readData1241 (readData1\_30\_OBUF)

OBUF:I->O 2.571 readData1\_30\_OBUF (readData1<30>)

----------------------------------------

Total 7.256ns (4.201ns logic, 3.055ns route)

(57.9% logic, 42.1% route)

=========================================================================

Cross Clock Domains Report:

--------------------------

=========================================================================

Total REAL time to Xst completion: 8.00 secs

Total CPU time to Xst completion: 7.65 secs

-->

Total memory usage is 4506632 kilobytes

Number of errors : 0 ( 0 filtered)

Number of warnings : 1 ( 0 filtered)

Number of infos : 2 ( 0 filtered)